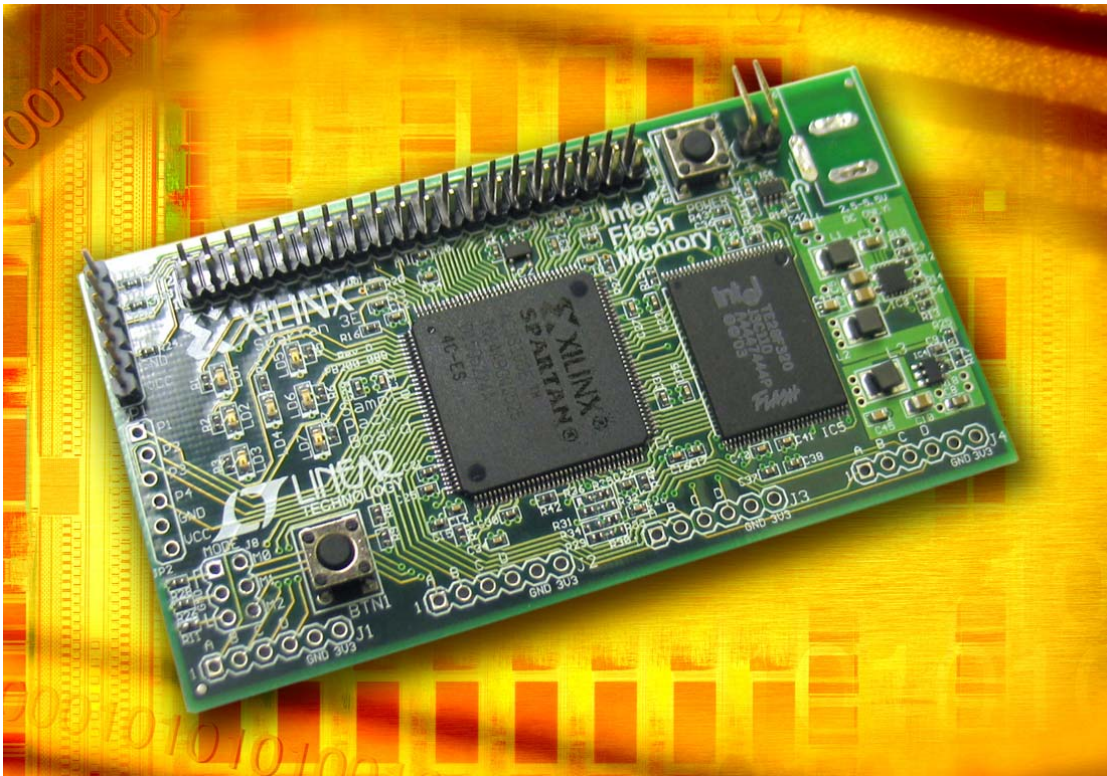


Xilinx Spartan-3E FPGA Sample Pack User's Guide





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	Version	Revision
11/10/05	1.0	Initial Xilinx Release

About this Guide

This user guide describes the components and operation of the Spartan-3E Sample Pack Board

Guide Contents

This manual contains the following chapters:

- Chapter 1: Getting Started
- Chapter 2: Parallel NOR Flash
- Chapter 3: Clock Sources
- Chapter 4: Switches and LEDs
- Chapter 5: FPGA Configuration Modes and Functions
- Chapter 6: JTAG Programming/Debugging Ports
- Chapter 7: Power Distribution
- Chapter 8: Expansion Connectors and Boards
- Appendix A: Board Schematics and Gerber Files
- Appendix B: Reference Material for Major Components

Getting Started

Introduction

The Xilinx Spartan-3E Sample Pack is a demonstration platform intended for you to become familiar with the new features and availability of the Spartan-3E FPGA family.

For a comprehensive development platform including a 500K-gate FPGA, evaluation versions of Xilinx ISE and Embedded Development Kit (EDK), and more, purchase a Spartan-3E Starter Kit. Please visit www.xilinx.com/s3eboards for more details.



Figure 1.1: Spartan-3E Starter Kit

Key Components and Features

Figure 1-2 shows the Spartan-3E Sample Pack board block diagram, which includes the following components and features:

- 100,000-gate Xilinx Spartan-3E XC3S100E FPGA in a 144-Thin Quad Flat Pack package (XC3S100E-TQ144)
 - 2,160 logic cell equivalents
 - Four 18K-bit block RAMs (72K bits)
 - Four 18x18 pipelined hardware multipliers
 - Two Digital Clock Managers (DCMs)
- 32Mbit Intel StrataFlash
- A 40-pin expansion connection port to gain access to the Spartan-3E FPGA
- Four 6-pin expansion connector ports to extend and enhance the Spartan-3E Sample Pack
 - Compatible with Digilent, Inc. peripheral boards
 - <http://www.digilentinc.com/products/Peripheral.cfm>
- 7 Light Emitting Diodes (LEDs)
- 50MHz Crystal Oscillator Clock Source
- Power Regulators

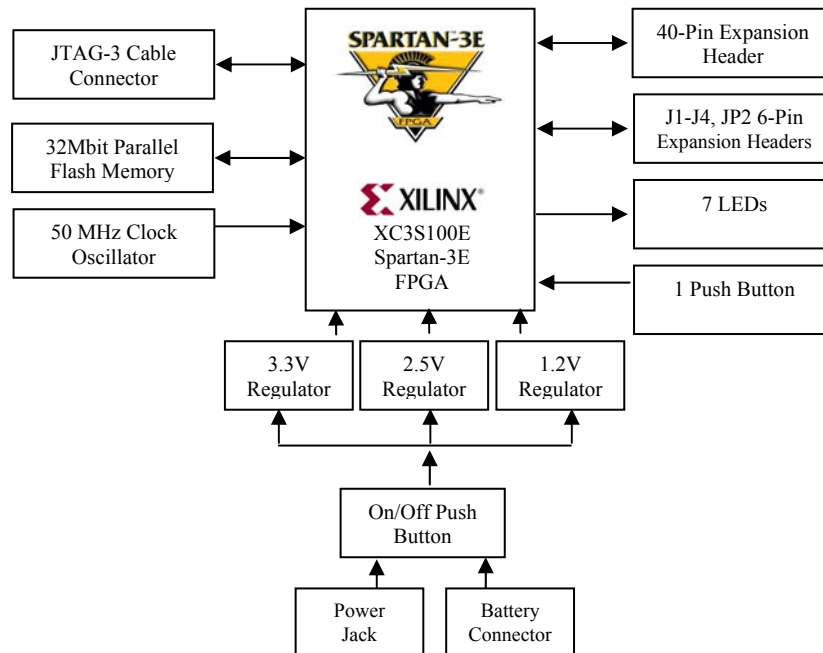


Figure 1-2: Xilinx Spartan-3E Sample Pack Board Block Diagram

Component Locations

Figure 1-3 indicates the component locations of a fully populated board. Note that some components are optional and can be added to increase the functionality of the board.

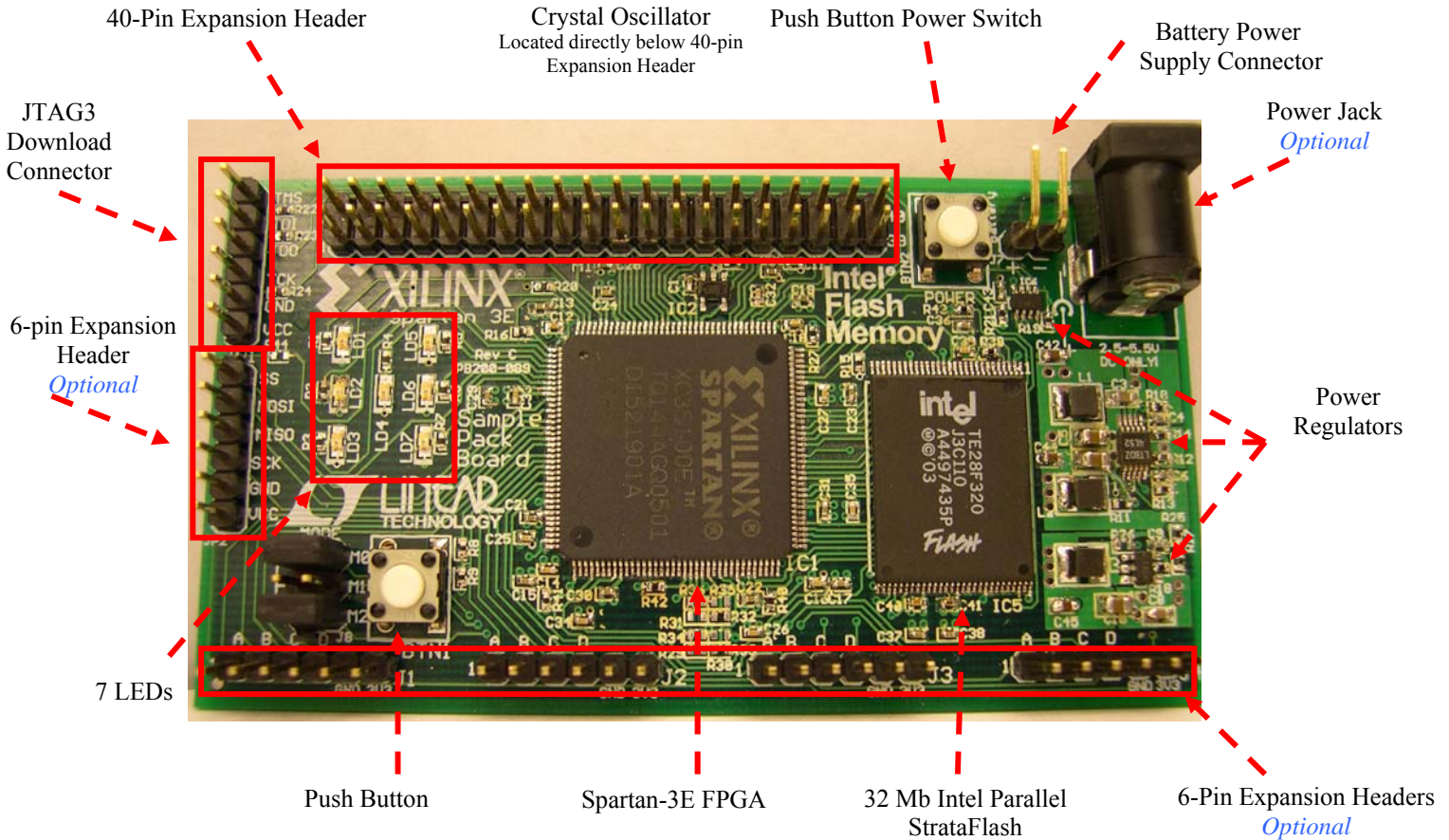


Figure 1-3: Xilinx Spartan-3E Sample Pack Board (Top Side)

Optional Components

A supplemental \$15 accessory pack is available to give customers additional options for expansion and programming. The accessory pack contains:

- JTAG3 Programming Cable
- Wall Power Supply (100V-220V, 50-60Hz)
- Wall Power Jack
- 6 pin expansion headers

For more information visit www.digilentinc.com/s3eaccessory

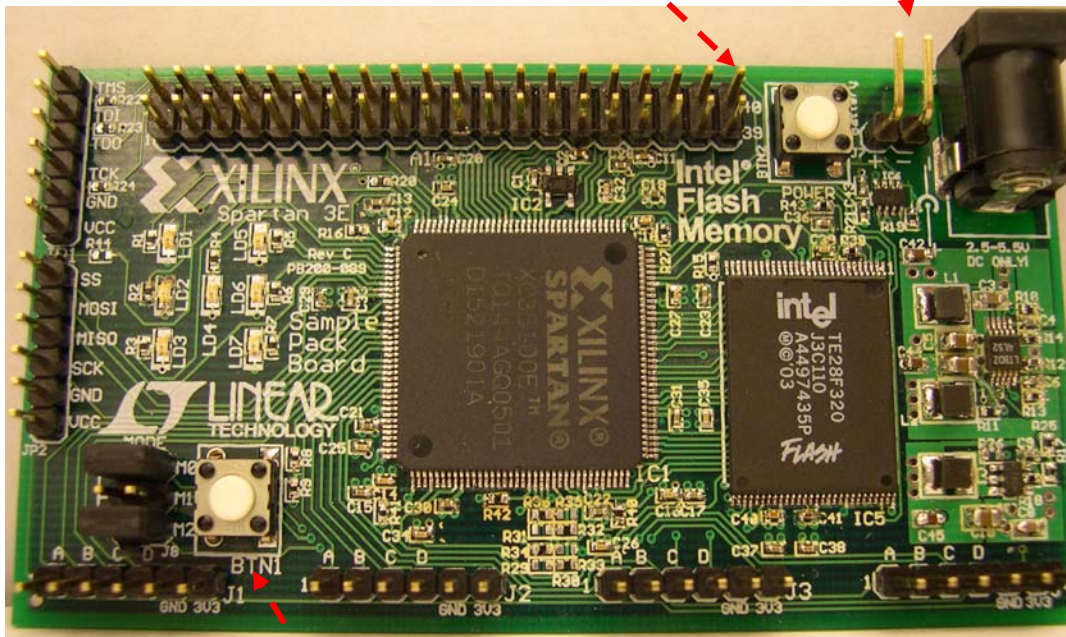


Powering Up the Board for the First Time

1. Connect Power to the Board
 - a. Connect positive and negative terminals on +5V supply
2. Initialize FPGA
 - a. Press power switch to apply power to the board
 - b. The “circling lights” design is automatically loaded into the FPGA from the Intel® StrataFlash and displayed on the LEDs
3. Exercise MultiBoot Feature
 - a. Press the momentary MultiBoot pushbutton to load a second design – the “Roll the Dice” game
 - b. Press switch again for another roll

1. Attach Power to Power Supply Connector

2. Power On / Initialize FPGA



3. Press MultiBoot Switch

Parallel NOR Flash

The Spartan-3E Sample Pack board has 32Mbit of parallel NOR flash used to configure the Spartan-3E FPGA in Byte-Peripheral Interface (BPI) mode. Additionally, the Intel StrataFlash can be used to store executable software code, user data, multiple FPGA configurations and copy protection methods. The StrataFlash is setup for x8 read / write operation and optionally x16 read operations from the Intel StrataFlash.

Refer to Chapter 5, “FPGA Configuration Modes and Functions” for more information on programming the Intel StrataFlash.

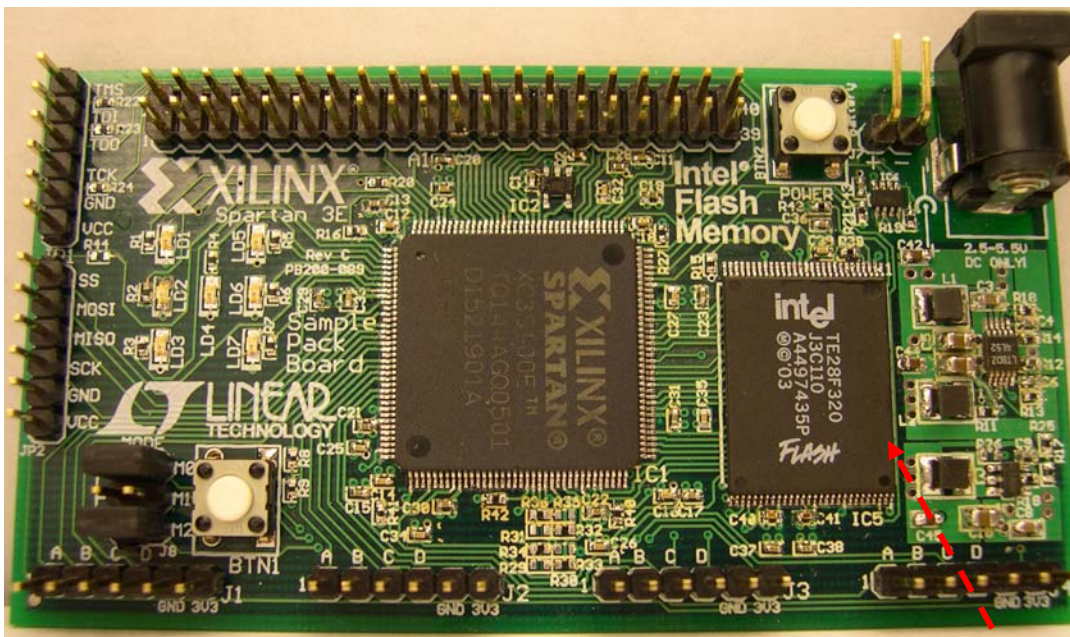


Figure 2-1. Intel StrataFlash Location

32 Mb Intel Parallel StrataFlash

Address Bus Connections

Table 2-1: External Flash Address Buss Connections to the Spartan-3E FPGA

Address Bit	FPGA Pin	A1 Expansion Connector Pin
A21	P83	-
A20	P44	-
A19	P67	-
A18	P68	-
A17	P70	-
A16	P74	-
A15	P75	-
A14	P76	-
A13	P77	-
A12	P81	-

A11	P82	-
A10	P85	-
A9	P86	-
A8	P87	-
A7	P88	-
A6	P91	-
A5	P92	14
A4	P93	12
A3	P94	10
A2	P96	8
A1	P97	6
A0	P98	4

Write Enable and Output Enable Control Signals

Table 2-2: Flash Control Signal Connections to Spartan-3E FPGA

Signal	FPGA Pin
OE#	P105
WE#	P103

Flash Data Signals, Chip Enables and Byte Enables

Table 2-3: External Flash Control Signal Connections to Spartan-3E FPGA

Signal	FPGA Pin
DB15 (input only)	P114
DB14 (input only)	P111
DB13 (input only)	P107
DB12 (input only)	P101
DB11 (input only)	P95
DB10 (input only)	P89
DB9 (input only)	P84
DB8 (input only)	P78
DB7	P50
DB6	P51
DB5	P52
DB4	P53
DB3	P54
DB2	P58
DB1	P59
DB0	P63
BYTE	P106
CE2	GND
CE1	GND
CE0	P104

Clock Source

The Spartan-3E Sample Pack board has a Linear Technology © LTC6905 Crystal Oscillator set to 50MHz. Use the 50MHz clock frequency as is or derive other frequencies using the FPGAs Digital Clock Managers (DCMs).

- Using Digital Clock Mangers (DCMs) in Spartan-3 Generation FPGAs
<http://www.xilinx.com/bvdocs/appnotes/xapp462.pdf>

Table 3-1: Clock Oscillator Source

Oscillator Source	FPGA Pin
50 MHz (IC2)	P122

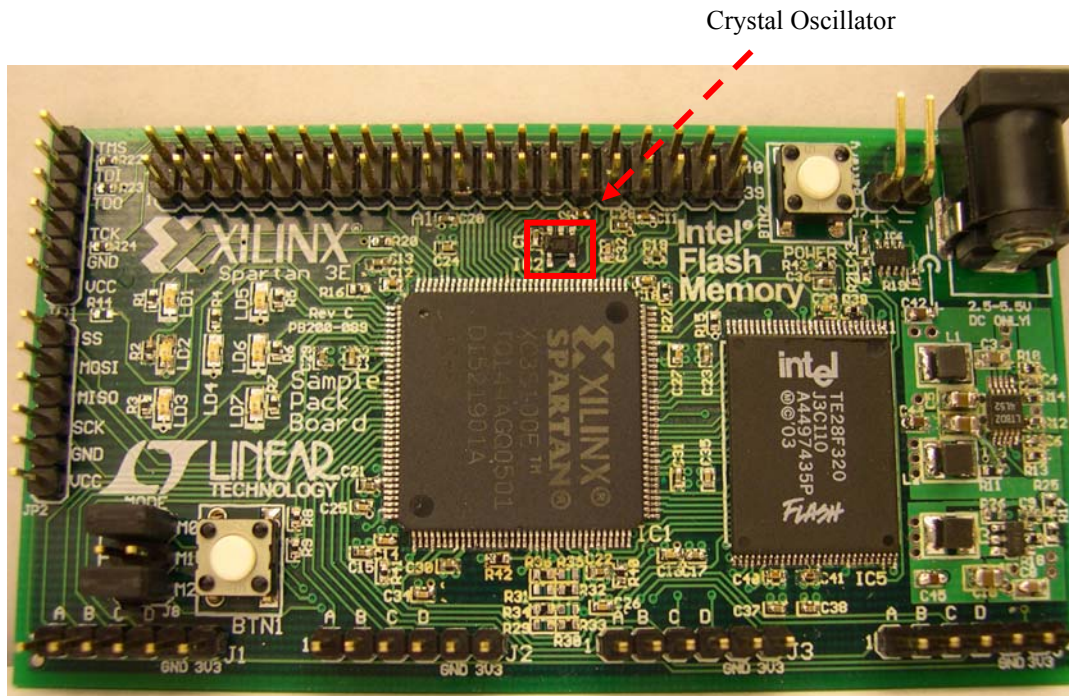


Figure 3-1. Crystal Oscillator Location

Switches and LEDs

Power Switch

The Spartan-3E Sample Pack board has a push button power switch. Pressing the power switch will alternately power on or power off the board.

Table 4-1: Push Button Switch Connections

Push Button	BTN2 (On/Off)
Board/FPGA Pin	LTC2950 (IC6) Pin 2 & 4

Multi-Use Switch

A multi-use push button switch is used in the default board designs to enable MultiBoot (see Chapter 5, *Sample Pack Default Designs* for more details). Depressing the switch generates a Logic High on the associated FPGA pin.

Table 4-2: Push Button Switch Connections

Push Button	BTN1 (MultiBoot)
Board/FPGA Pin	FPGA Pin - P18

LEDs

The Spartan-3E Sample Pack board has 7 individual surface-mount LEDs located to the left of the FPGA. The LEDs are labeled LD7 through LD1 and are laid out in an “H” pattern to mimic a Die used in a Dice game.

Table 4-3: LED Connections to the Spartan-3E FPGA

LED	LD7	LD6	LD5	LD4	LD3	LD2	LD1
FPGA Pin	P7	P5	P4	P3	P2	P43	P142

The cathode of each LED connects to ground via a 390Ω resistor. To light an individual LED, drive the associated FPGA control signal High.

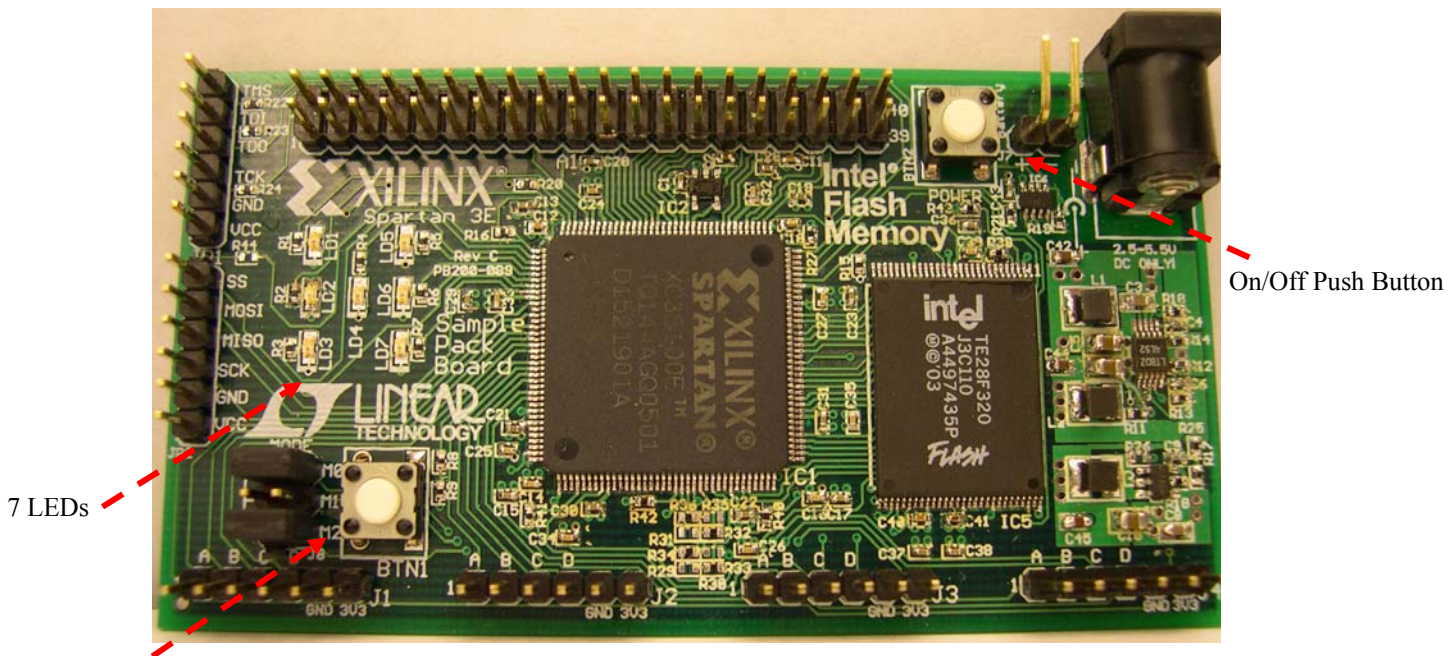


Figure 4-1. Switches and LED Location

Multi Use Push Button

FPGA Configuration Modes and Functions

The Spartan-3E FPGA family supports a Byte-Peripheral Interface (BPI) configuration mode allowing the use of low cost commodity parallel NOR flash for FPGA configuration. Additionally, unused memory space in the flash can be used for other functions such as software code storage.

Sample Pack Default Designs

A new feature in the Spartan-3E FPGA family is MultiBoot, which allows BPI reconfiguration of the FPGA in either a top boot or bottom boot configuration scheme. For example, the initial Sample Pack configuration uses BPI-UP mode. Once MultiBoot has been triggered (in this case by depressing BTN1) the FPGA will configure in BPI-DN mode. For more details on MultiBoot refer to the Spartan-3E datasheet.

The sample pack board contains two designs; Circling LEDs and “Dice” game. The mode pins on the board are setup such that the FPGA first configures in BPI-UP mode with the Circling LEDs design (which strobes the LEDs in a circular pattern). BTN1 is used to trigger the FPGA to reconfigure in BPI-DN mode with the dice game (which mimics “rolling a die” as seen on the LEDs). Table 5.1 lists the Memory Map of the designs stored on the Intel StrataFlash. The source codes for both of these designs are included on the Sample Pack Resource CD.

Table 5.1: Memory Map of Intel StrataFlash on Sample Pack

Name	Memory Block	Start Address	End Address	Total Space
Unused	0 (lsb)	0x000000	0x00E422	57.04 KBytes
Circling LED design	0 (msb)	0x00E423	0x1FFFFF	70.96 KBytes
Unused Space	1-6	0x020000	0x0DFFFF	768 KBytes
Dice Game	7 (lsb)	0x0E0000	0xF1BDC	70.96 KBytes
Unused Space	7 (msb)	0x0F1BDD	0xFFFFF	57.04 KBytes
User Space	8-31	0x100000	0x3FFFFFF	3 MBytes

Creating a Configuration File

When a configuration bitstream (*.bit) is created in ISE, the user must ensure that the startup clock is CCLK in the bitgen options. A binary configuration file (*.bin) must be generated for BPI-up configuration using the following promgen command in any command window. In the example demowithstartup.bit, the configuration file is used to generate the bitstream.bin binary configuration file setup for BPI-up configuration using the following command line:

```
promgen -w -p bin -c FF -o circlingLEDs_bpi_up.bin -u 0
demowithstartup.bit
```

In the example dice.bit, the configuration file is used to generate the dice_bpi_down.bin binary configuration file for BPI-up mode using the following command line:

```
promgen -w -p bin -c FF -o dice_bpi_down.bin -d 0xFFFFF dice.bit
```

Customized Flash Writer for Sample Pack

Data is loaded into the flash device using EDK and MicroBlaze, a 32-bit soft-core processor. The EDK software normally includes a flash writer to write to parallel NOR flash while getting the configuration data from the JTAG port as shown in Figure 5.1. A smaller customized flash writer was

created to fit within the 4 block RAMs of the XC3S100E as shown in Figure 5.2 and is located on the Sample Pack Resource CD. Normally the EDK flash writer requires 32KByte of FPGA memory. The customized Sample Pack flash writer uses 8KByte of FPGA memory.

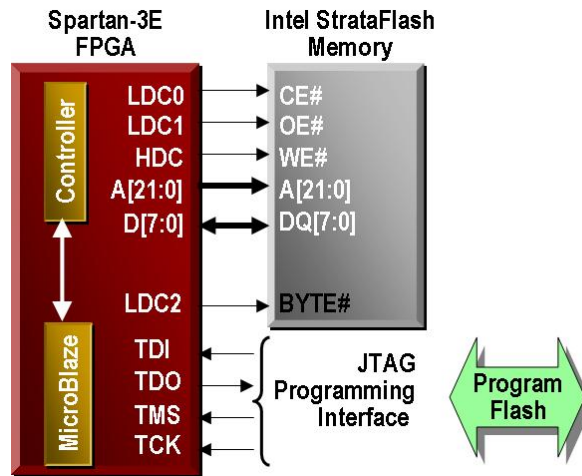


Figure 5.1. Block Diagram shows StrataFlash being programmed using the FPGA with a MicroBlaze controller to retrieve data from the JTAG port.

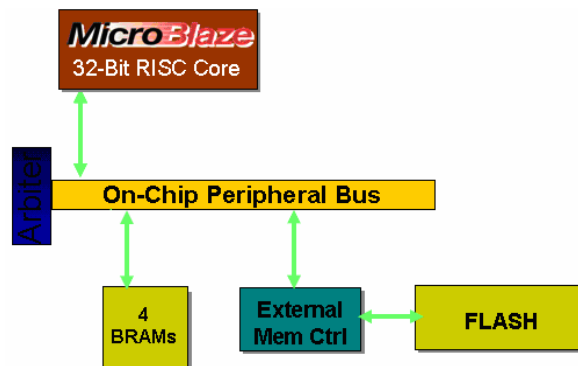


Figure 5.2. MicroBlaze System Block Diagram

Configuring the Flash Memory

Once the configuration files have been created, you can start storing the binary configuration files in the flash using the custom flash writer software. You must install at least versions ISE 7.1i Service Pack 4 and EDK 7.1i Service Pack 2 to continue. The flash writer software must be configured to tell the programmer what data files you want to program into the flash device. The settings must be set in the `flash_params.tcl` file which can be found in the directory `<project_directory>/flashwriter/etc/`. The `FLASH_FILE` parameter must be set to the complete path of the binary file that is to be programmed into the flash. Next the `FLASH_PROG_OFFSET` parameter must be set to the offset within the flash that the file needs to be programmed.

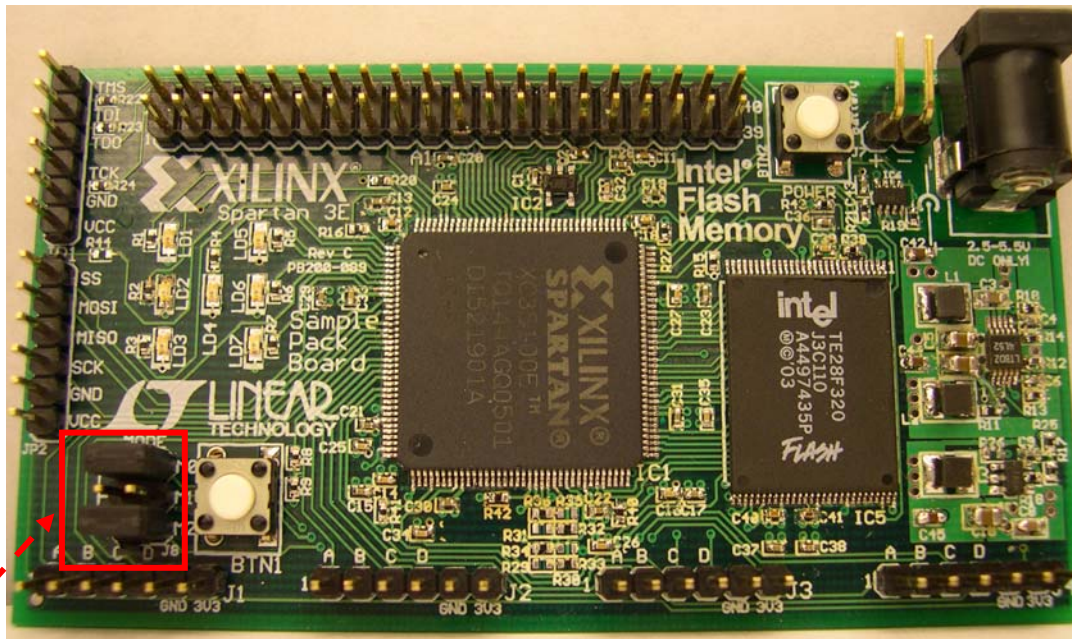
Note that the flash writer software will erase 128Kbyte blocks at one time therefore that could be used for partitioning data within the flash. Refer to Table 5.1 for details on the default programs stored in the flash.

1. Open the provided EDK project flashwriter in Xilinx Platform Studio.
2. Within a text editor, verify that the `flash_params.tcl` file has the correct file to download and correct offset.
3. Connect the JTAG cable to Spartan-3E Sample Pack board on JP2.
4. Go to the 'Tools' menu and click on 'Generate Libraries and BSP' to generate the software libraries that the flash writer utilizes.
5. Go to the 'Tools' menu and click on 'Download' to download the Flashwriter hardware to the Spartan-3E device on the Sample Pack board.
6. Go to the 'Tools' menu and click on 'Xilinx Command Shell' to open a command prompt.
7. In the new Command Shell, type `xmd -tcl flashwriter.tcl` to start the flash writer software.
8. Note that the flash writer software may take a few minutes depending on the size of the file to program. An example of the status output is shown in `output.txt`.

Configuration Mode Pins

Currently, the board default configuration is BPI Up mode as set by JP8. You can program the board via a JTAG3 Cable or Xilinx Parallel Cable 3 (PC3) cable inserted in JP1 without any jumpers/modifications to the Configuration Mode Pins.

To customize the mode settings you must first cut the trace on the back of the board between Block J8 Pins 1 & 2, and Block J8 Pins 5 & 6 as seen in Figure 5.4.



Configuration Mode Pins

Figure 5.3. Location of Configuration Mode Pins

Table 5.2: Pinout for J8, Mode Select Jumper Block

Schematic Name	FPGA Pin
MODE0 (M0)	P62
MODE1 (M1)	P60
MODE2 (M2)	P57

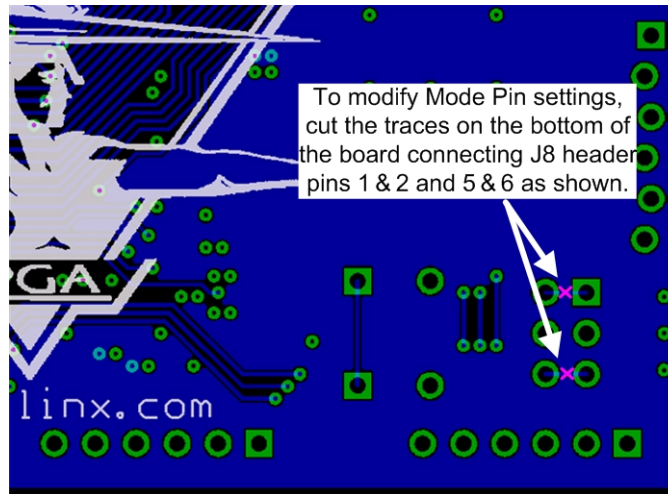


Figure 5.4. Mode Pin Traces on Back of Board

Three board pins - M2, M1 and M0 select the desired configuration mode as listed in Table 5.3. Column 2 lists out the pin settings as per the FPGA Device Data Sheet. On the board however, the jumper settings are opposite as per Column 3. For instance, to have the board in Slave Parallel mode you would place a jumper only on jumper M1.

Table 5.3: Programming Settings – User Customized

Programming Options	M[2:0] FPGA Pin Settings as per Data Sheet	M[2:0] Jumper Settings on Board
Master Serial	000	111
SPI	001	110
BPI Up	010	101
BPI Down	011	100
Slave Parallel	101	010
JTAG	110	001
Slave Serial	111	000

JTAG Programming/Debugging Ports

The Spartan-3E Sample Pack board includes a JTAG programming and debugging chain. Both the Spartan-3E FPGA and the Parallel Flash are part of the JTAG chain. Additionally, a JTAG header is available for driving the JTAG signals from various supported JTAG download and debugging cables.

JTAG Header (JP1)

The JP1 JTAG header is located toward the top left edge of the board. A JTAG cable can be fitted directly over the JP1 header stake pins. When properly fitted, the cable is perpendicular to the board. The JP1 header also supports the Xilinx Parallel Cable 3 (PC3) download/debugging cable.

JTAG3 Cable
Connector
JP1

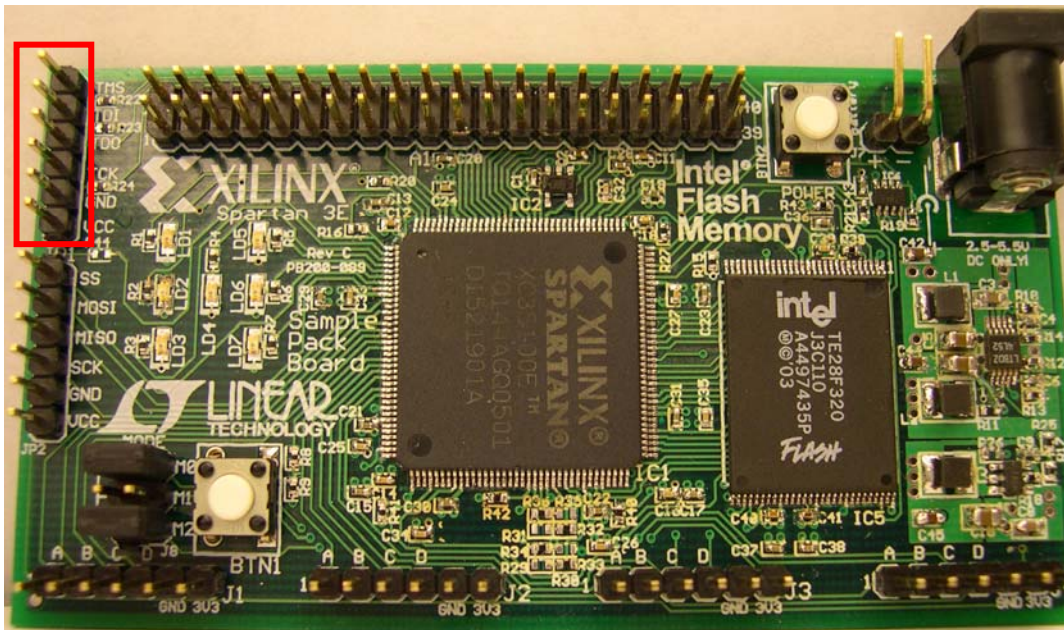


Figure 6-1. JTAG Connector Location

Power Distribution

Voltage Regulators

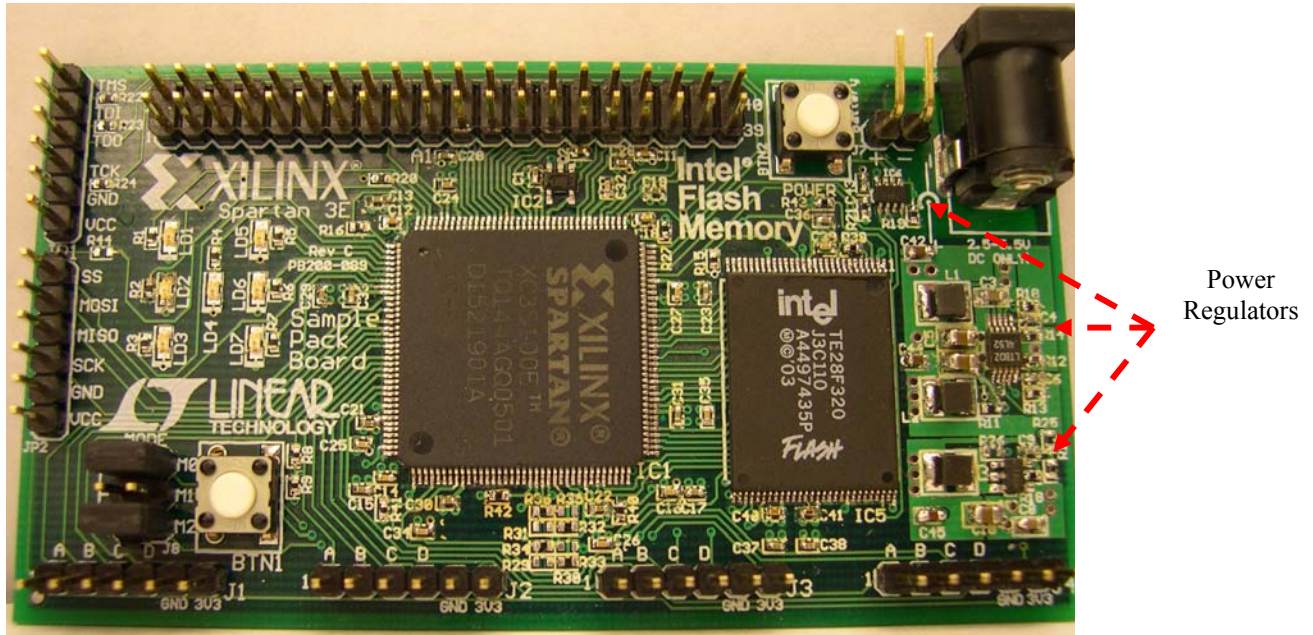


Figure 7-1. Voltage Regulator Location

There are multiple voltages supplied on the Spartan-3E Sample Kit Board, as summarized in Table 7-1.

Table 7.1: Voltage Supplies and Sources

Voltage	Source	Supplies
+3.3V DC	Linear Technology LTC3407-2	2.5V and 1.2V regulators V _{CCO} supply input for all FPGA I/O banks Most components on the Board
+2.5V DC	Linear Technology LTC3406B	V _{CCAUX} supply input to FPGA
+1.2V DC	Linear Technology LTC3407-2	V _{CCINT} supply input to FPGA

A 3.3V regulator provides power to the inputs of the 2.5V and 1.2V regulators. Similarly, the 3.3V regulator feeds all the V_{CCO} voltage supply inputs to the FPGAs I/O banks and powers most of the components of the board.

The 2.5V regulator supplies power to the FPGAs V_{CCAUX} supply inputs. The V_{CCAUX} voltage input supplies power to the Digital Clock Managers (DCMs) within the FPGA and supplies some of the I/O structures. In specific, all of the FPGA/s dedicated configuration pins, such as DONE, PROG_B, CCLK, and the FPGAs JTAG pins, are powered by V_{CCAUX} supply has current shunt resistor to prevent reverse current.

Expansion Connectors and Boards

Expansion Connectors

The Spartan-3E Sample Pack board has one 40-pin expansion header labeled A1 at the top portion of the board - Note only 35 pins of the A1 header are actually connected to the FPGA. Additionally a 6-pin expansion header can be inserted into J1, J2, J3, and J4.

Header pins can be inserted into the J1-J4 thru-holes to expand the capabilities of the Sample Pack. For more information see section “Expansion Boards” later in this chapter.

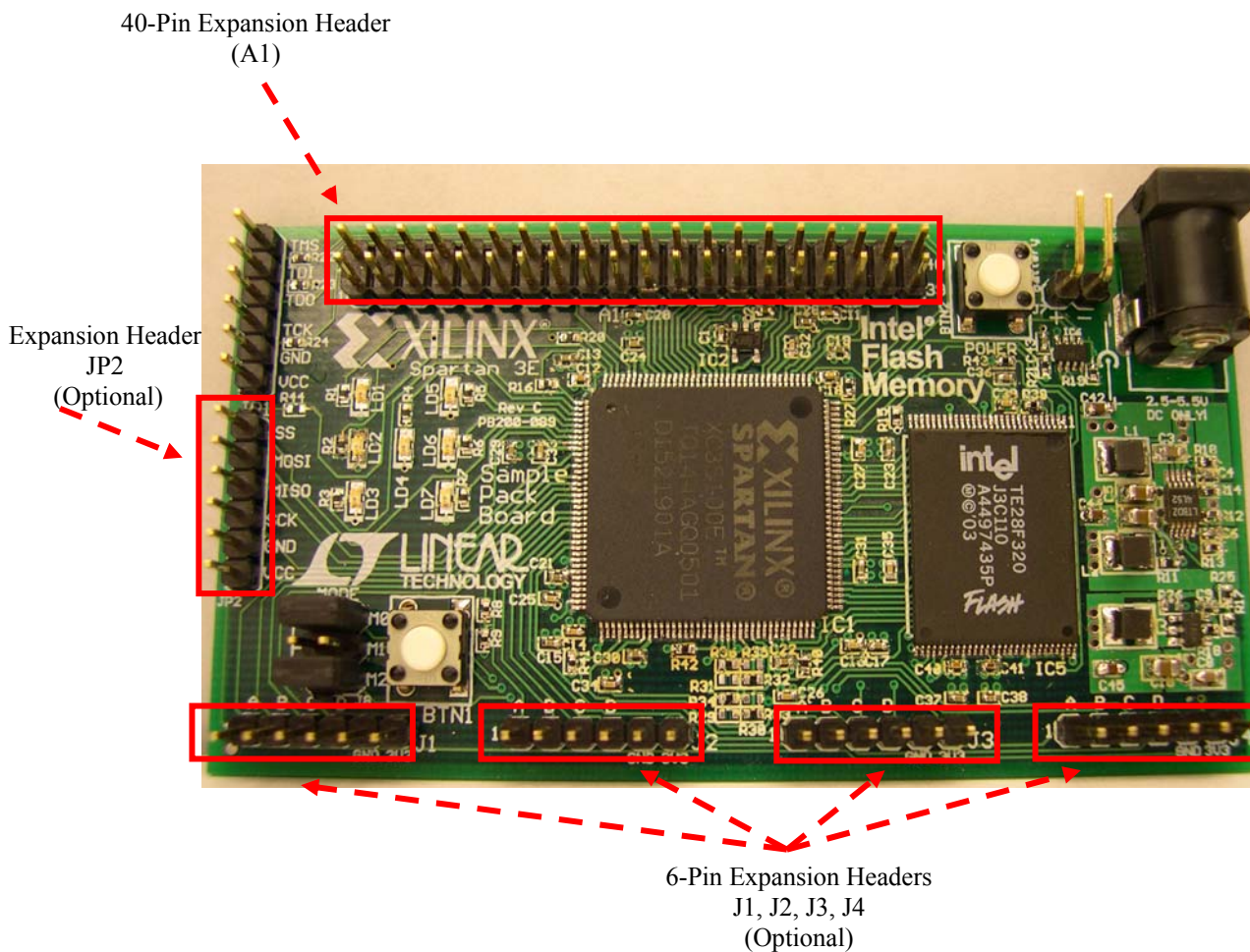


Figure 8-1. Expansion Header Locations

Table 8-1: Pinout for A1 Expansion Connector

Schematic Name	FPGA Pin	Connector		FPGA Pin	Schematic Name
GND		1	2		VU (+5V)
V _{CC} (+3.3V)	V _{CC0} (all banks)	3	4	P98	ADR0
DB0	P63	5	6	P97	ADR1
DB1	P59	7	8	P96	ADR2
DB2	P58	9	10	P94	ADR3
DB3	P54	11	12	P93	ADR4
DB4	P53	13	14	P92	ADR5
DB5	P52	15	16	P140	WE-A
DB6	P51	17	18	P139	OE-A
DB7	P50	19	20	P135	CSA
LSBCLK	P134	21	22	P132	MA1-DB0
MA1-DB1	P131	23	24	P130	MA1-DB2
MA1-DB3	P129	25	26	P128	MA1-DB4
MA1-DB5	P126	27	28	P125	MA1-DB6
MA1-DB7	P124	29	30	P123	MA1-ASTB
MA1-DSTB	P113	31	32	P117	MA1-WRITE
MA1-WAIT	P116	33	34	P56	MA1-RESET
MA1-INT	P112	35			

Table 8-2: Pinout for J1 Expansion Connector

Schematic Name	FPGA Pin	Connector
J1 A	P14	1
J1 B	P15	2
J1 C	P16	3
J1 D	P17	4
GND		5
VCC3V3		6

Table 8-3: Pinout for J2 Expansion Connector

Schematic Name	FPGA Pin	Connector
J2 A	P20	1
J2 B	P21	2
J2 C	P22	3
J2 D	P23	4
GND		5
VCC3V3		6

Table 8-4: Pinout for J3 Expansion Connector

Schematic Name	FPGA Pin	Connector
J3 A	P25	1
J3 B	P26	2
J3 C	P29	3
J3 D	P32	4
GND		5
VCC3V3		6

Table 8-5: Pinout for J4 Expansion Connector

Schematic Name	FPGA Pin	Connector
J4 A	P33	1
J4 B	P34	2
J4 C	P35	3
J4 D	P40	4
GND		5
VCC3V3		6

Table 8-6: Pinout for JP2 Expansion Connector

Schematic Name	FPGA Pin	Connector
P1 (input only)	P6	1
P2 (input only)	P10	2
P3	P8	3
P4 (input only)	P12	4
GND		5
VCC3V3		6

Expansion Boards

Numerous expansion boards plug into A1, J1, J2, J3, J4, connectors from Digilent Inc. as listed below:

- Expansion Boards
 - <http://www.digilentinc.com/products/Accessory.cfm>
- 6-pin Expansion Boards
 - <http://www.digilentinc.com/products/Peripheral.cfm>

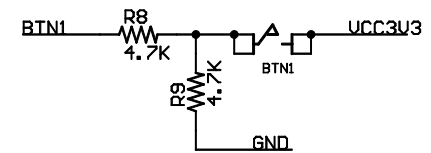
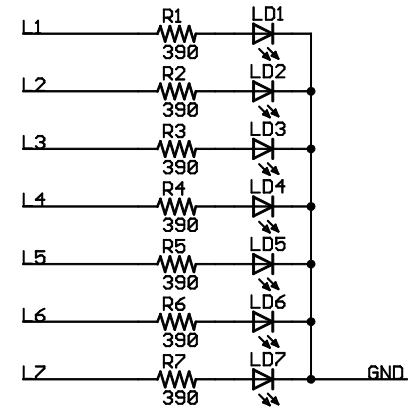
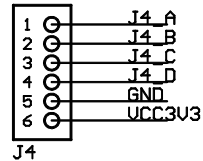
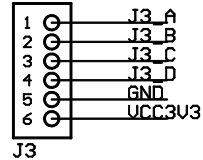
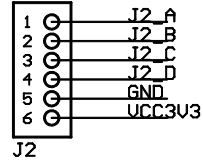
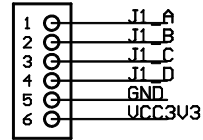
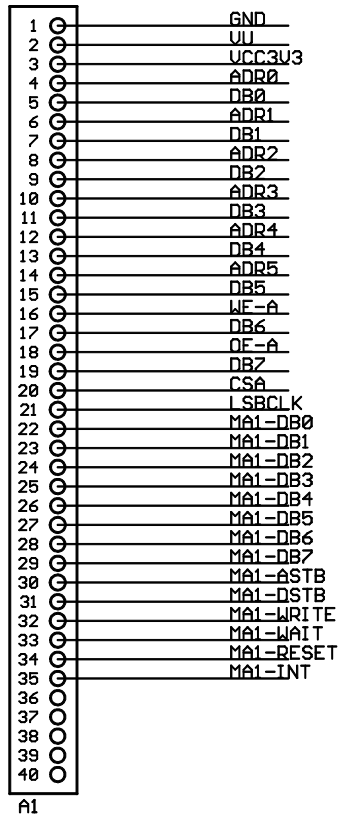
Table 8-7: Example of Expansion Boards from Digilent

Board	Application
A/D, D/A, Amplified Speaker	Signal Processing
H-Bridge, Servo Motor Control	Motor Control
UART, BNC, Wire Terminal, Open Collector Resistors, LEDs, Slide Switches	Computing / General Use

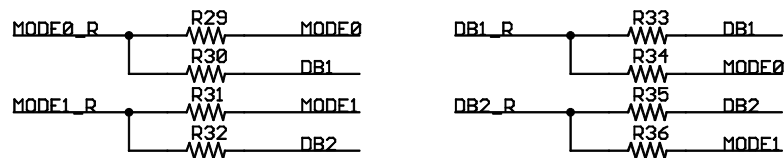


Board Schematic and Gerber Files

Offboard Connectors, LEDs and Button



0 ohm shunts for XC3S100E Revision A/B changes



Rev A: Load R30, R32, R34, R36
Rev B: Load R29, R31, R33, R35

S3E Sample Pack Board		Engineer: CC
Digilent Inc. Copyright 2005		Author: GMA
TITLE: S3ESP		Rev: D.1
Document Number: 500-089		Sheet: 1/4
Release Date: 11/07/05		

SPARTAN 3E

Xilinx

Digilent Inc.

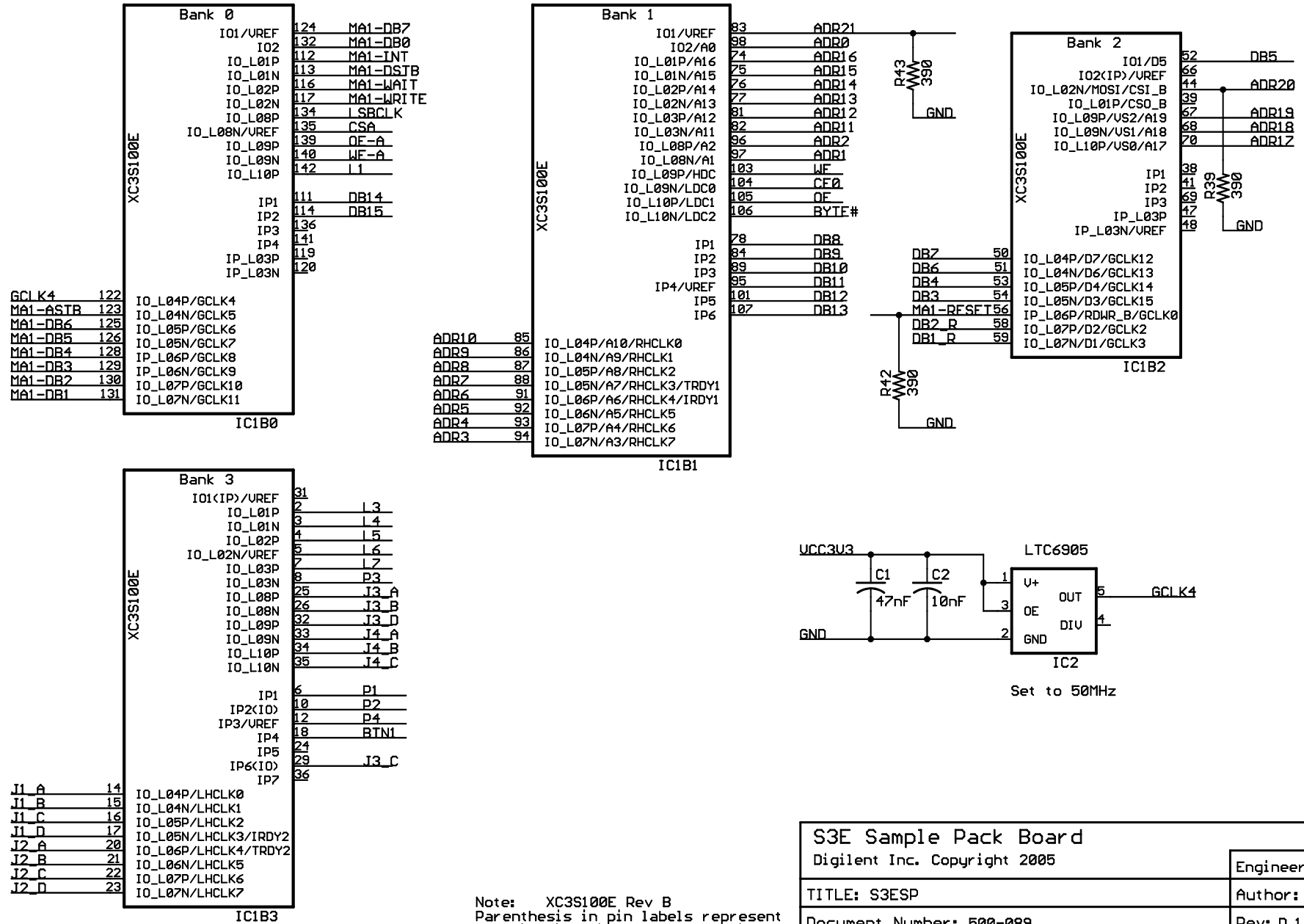
Linear Technology

Intel Stratflash

● FID1

● FID2

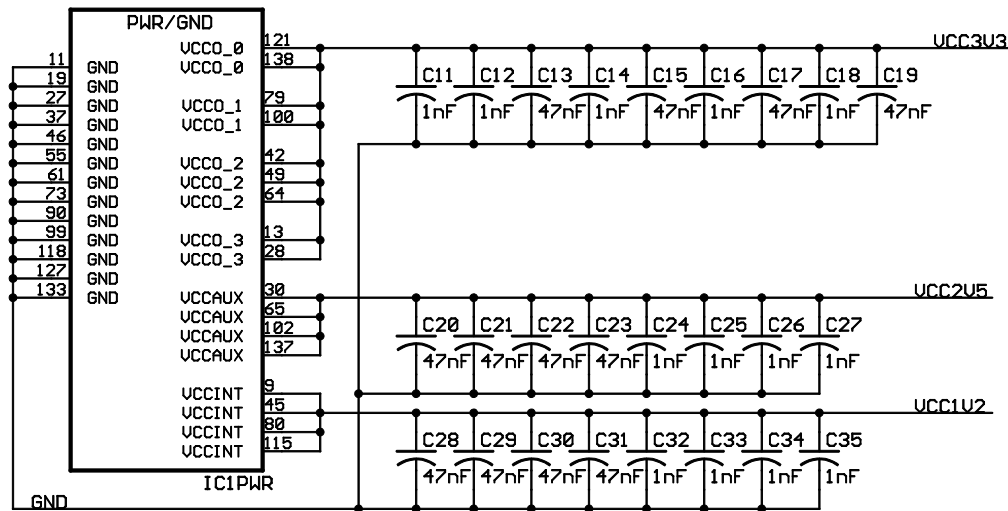
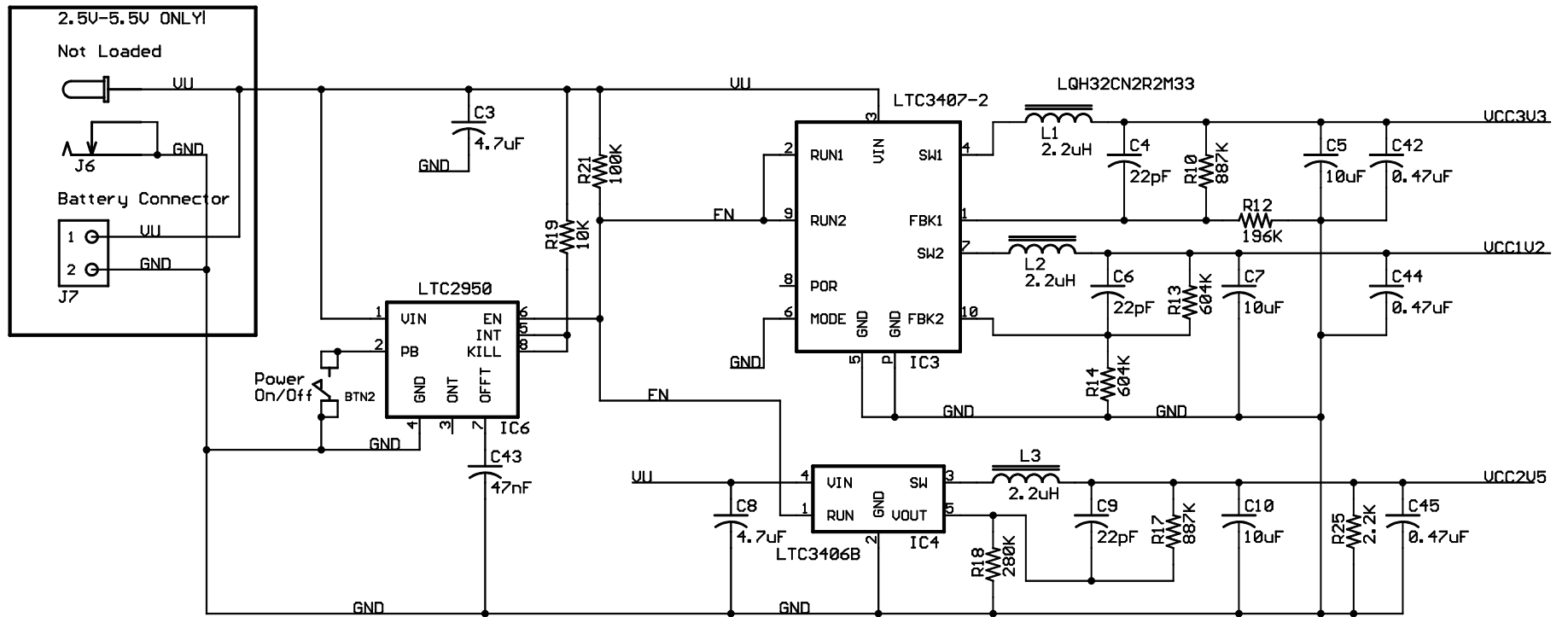
FPGA Connections and Oscillator



Note: XC3S100E Rev B
 Parenthesis in pin labels represent the pin direction on the 100 die
 IP6<IO> = 250<100>

S3E Sample Pack Board		Engineer: CC
Digilent Inc. Copyright 2005		Author: GMA
TITLE: S3ESP	Document Number: 500-089	Rev: D.1
Release Date: 11/07/05		Sheet: 2/4

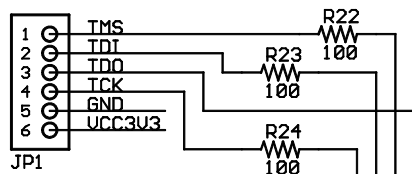
Power Supply, Regulators, FPGA Decoupling



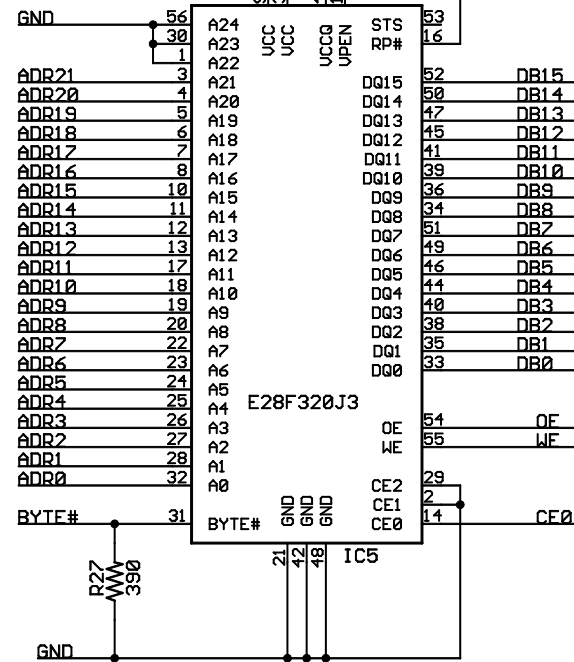
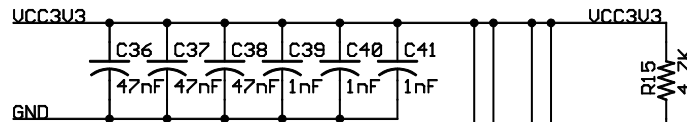
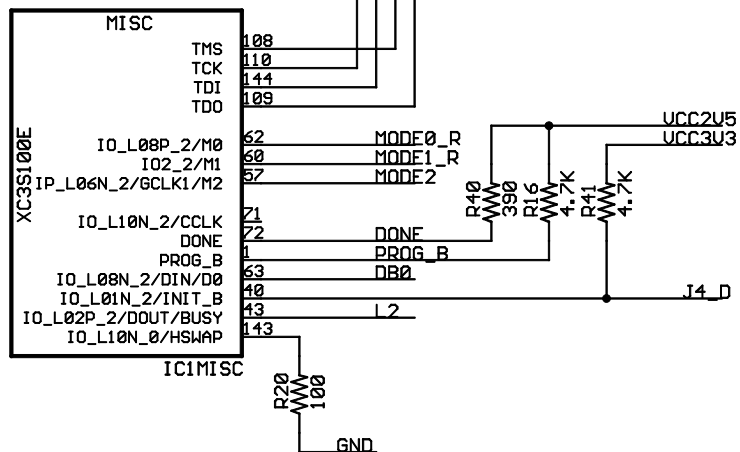
S3E Sample Pack Board		Engineer: CC
Digilent Inc. Copyright 2005		Author: GMA
TITLE: S3ESP		Rev: D.1
Document Number: 500-089		Sheet: 3/4
Release Date: 11/07/05		

JTAG, FPGA Programming and Intel StrataFlash

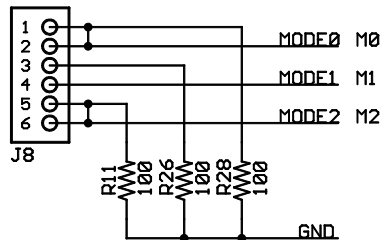
JTAG Header



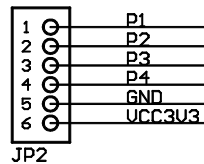
FPGA Programming Signals



Mode Select Jumper



Alternate Programming

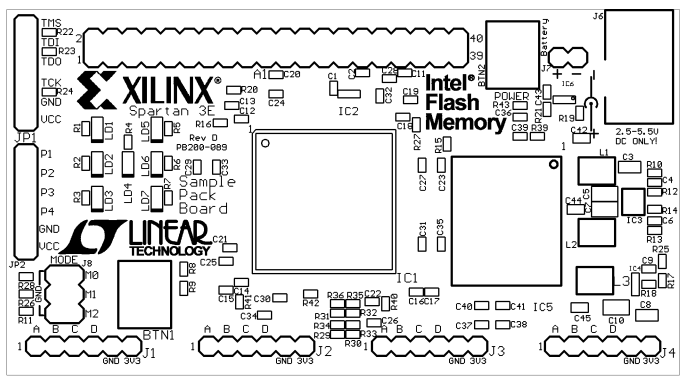


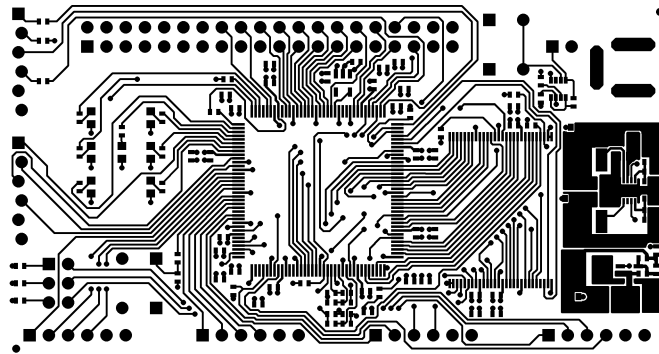
Default Mode BPI Incrementing

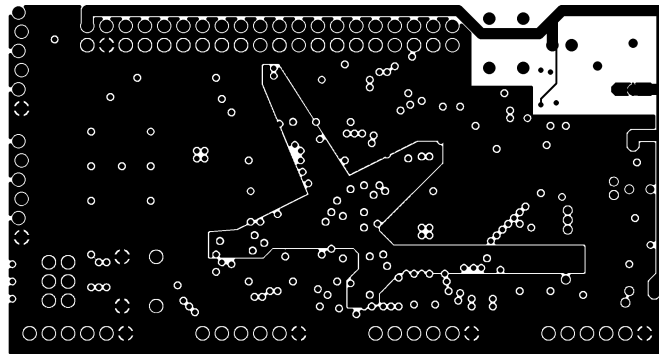
Notes:

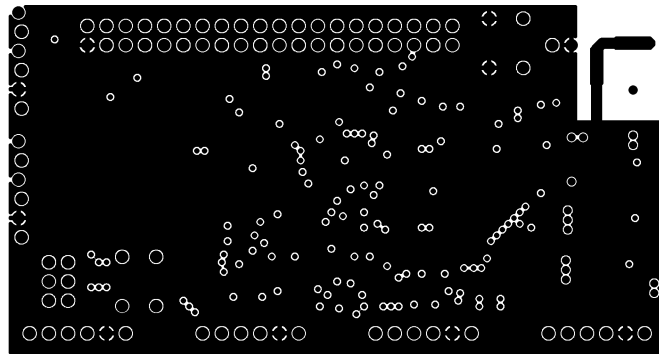
To change Mode settings, sever connections on J8 between pins 1 and 2, and also pins 5 and 6.

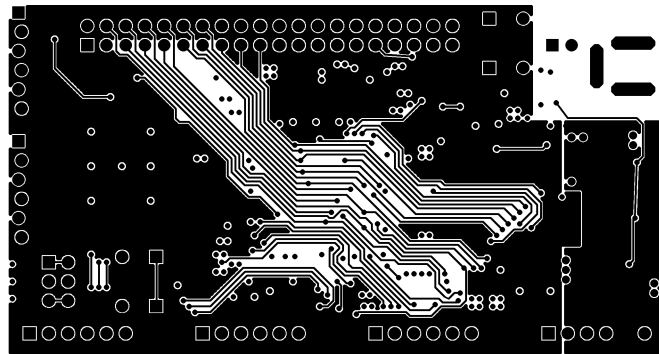
S3E Sample Pack Board		Engineer: CC
Digilent Inc. Copyright 2005		Author: GMA
TITLE: S3ESP		Rev: D.1
Document Number: 500-089		Sheet: 4/4
Release Date: 11/07/05		



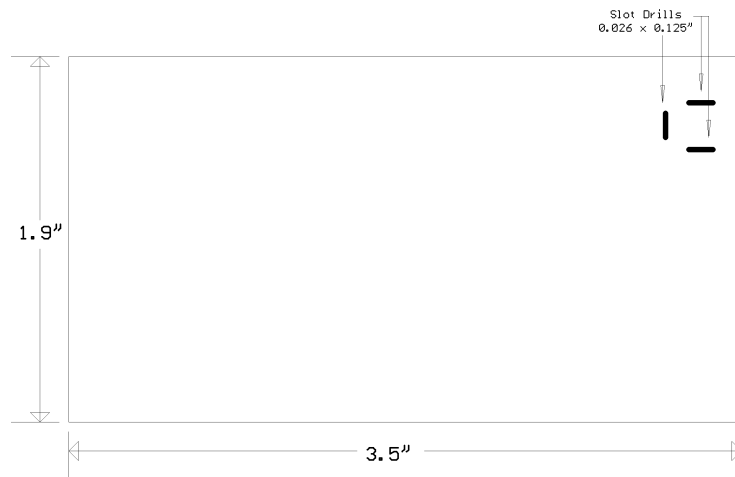












Reference Material for Major Components

Table B-1 lists the major components on the Spartan-3E Sample Kit Board, including full part numbers and links to complete device data sheets.

Device	Vendor	Part Number	Description/Data Sheet Link
FPGA	Xilinx, Inc	XC3S100E-4TQ144ES	Spartan-3E FPGA http://direct.xilinx.com/bvdocs/publications/ds312.pdf
Parallel Flash	Intel	28F320J3	Intel StrataFlash Memory (J3) http://www.intel.com/design/flcomp/prodbref/298044.htm
Voltage Regulators	Linear Technology	LTC3407-2, LTC3406	http://www.linear.com
Oscillator	Linear Technology	LTC6905-50	